Monthly Report for

12-Bit High Dynamic Range ADC

Reporting Period: 15 February 1998 to 15 March 1998

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Prepared for:

Gregory M. Nichols
Naval Research Lab
Code: 5725
4555 Overlook Ave., S.W.
Washington, D.C. 20375-5320

Submitted by:

Bert K. Oyama
TRW Space & Electronics Group
Electronic Systems & Technology Division
One Space Park
Redondo Beach, CA 90728

1.0 Technical Progress

During this reporting period, detailed layout of the ADC chip and final circuit simulations continued. The attached figure shows a plot of the partially completed chip layout. All signal path cell layouts have been completed. To address manufacturability issues, the chip floorplan was revised slightly, resulting in a reduction in overall chip size (by approx. 15%) to 4.9 mm x 4.5 mm. Critical blocks are currently being reviewed and layout revision recommendations generated. Block-to-block routing is in progress, and interconnect parasitics are being extracted to enable back-annotation of circuit simulation files. Critical signal paths are then re-simulated and circuit designs adjusted to optimize performance.

2. Plans for Next Reporting Period

During the next reporting period, the detailed chip layout and circuit simulations will be completed.

3. Financial Status

The attached table shows the forecasted versus actual expenditures for the Phase 1 program. At month-end February, 1998 we are showing a deviation from forecast of $5.4K (out of a cumulative actual of $486.3K, or about 1%). This is a reduction in forecast deviation of $21.6K (compared to month-end January), and is primarily the result of a return to normal headcount levels.

Table 1. Program Expenditures Forecast

Month	Monthly Total ($K)	Cumulative Total ($K)	Cumulative Actuals ($K)	Delta (Forecast - Actuals)
Jun-97	5.3	5.3	2.3	3.0
Jul-97	35.7	41.0	26.4	14.6
Aug-97	42.4	83.4	65.6	17.8
Sep-97	40.7	124.1	127.8	-3.7
Oct-97	81.1	205.2	203.6	1.6
Nov-97	58.4	263.6	268.1	-4.5
Dec-97	55.2	318.8	356.0	-37.2
Jan-98	89.1	407.9	434.9	-27.0
Feb-98	73.0	480.9	486.3	-5.4
Mar-98	75.7	556.6		
Apr-98	121.8	678.4		
May-98	64.6	743.0		
Jun-98	73.7	816.7		
Jul-98	103.4	920.1		
Aug-98	77.8	997.9		
Sep-98	64.9	1062.8		
Oct-98	72.2	1135.0		
Nov-98	54.0	1189.0		

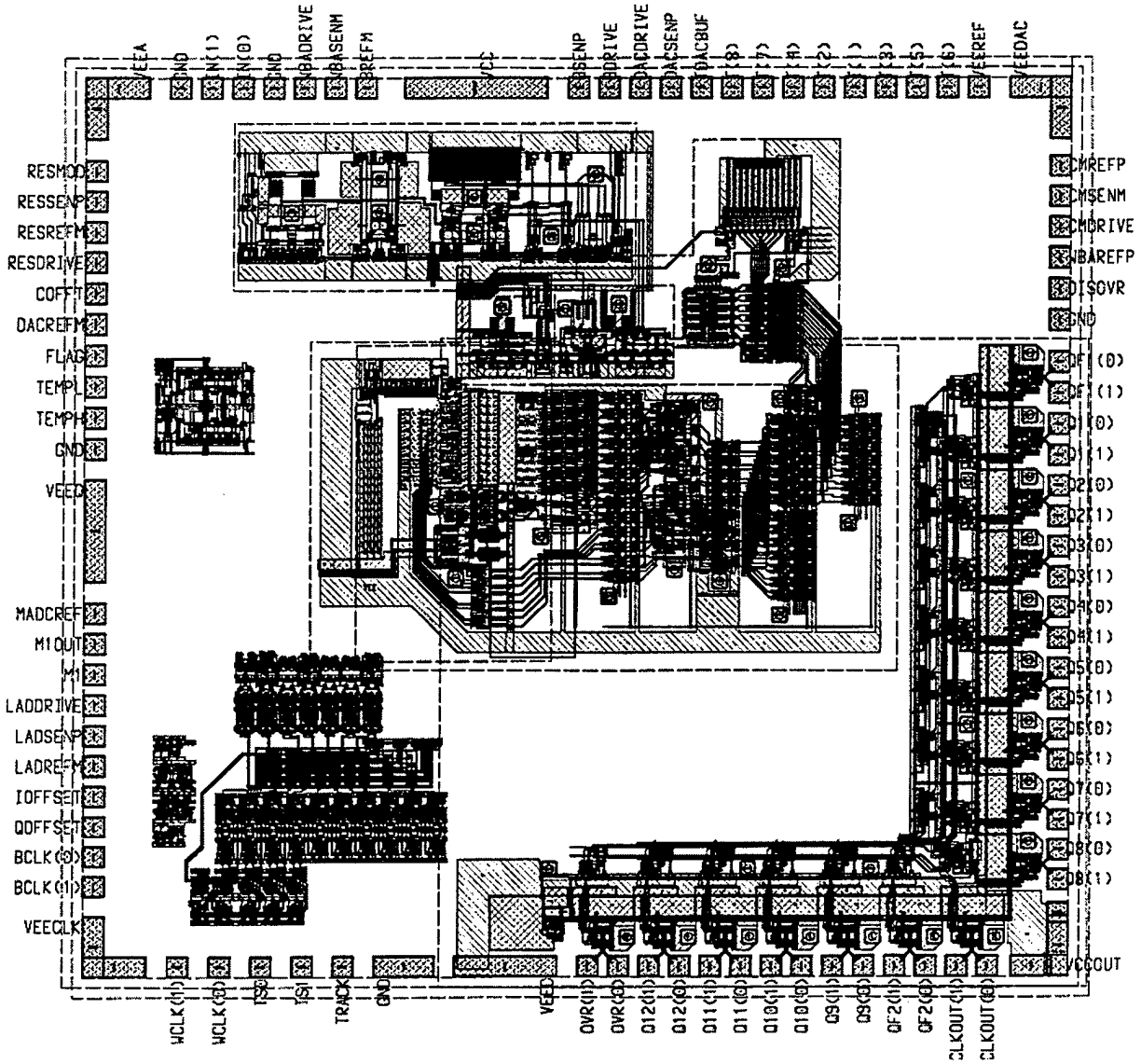

Figure 1. Plot of partially completed ADC chip layout.